ON THE NON-ORIENTED LINEAR ZONES MIGRATION THROUGH (100) SILICON WAFERS FOR POWER DEVICES FABRICATION

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Abstract. *Diodes of direct polarity with thermomigrated p-isolation walls had been produced. The high-power chips were made from n-type (100) silicon wafers. Non-oriented linear zones had complex shape. Novelled technology provides for high yield of chips with blocking voltage closely approaching to the theoretical prediction and current up to 250 A.*

1. INTRODUCTION

Lately glass-passivated silicon chips (thyristors, triacs, diodes etc) almost always displaced conventional rounded beveled structures in power silicon modules. One-sided passivation is preferable for these chips. These chips are fabricated using separation process so that blocking junctions are terminated on the topside of the chip [1]. Now the entire bottom surface of the chip is available for soldering. So heat sink is more effective, the process of chip control on a wafer is simplified etc.

To expose lower blocking p-n junction of every chip on upper side of the wafer the peripheral insulating p-wall around the perimeter of each chip is needed. To make this insulating p-walls solid-state diffusion process is used commonly. As acceptor dophant boron is used basically. This process has any well known drawbacks: variable p-dophant concentration across the wafer depth, area losses because of lateral diffusion, and a square-law dependency of diffusion time from required p-n junction depth. These dramatically enlarge the thermal budget of the high temperature wafer treatment, and eventually limit the thickness of the processed wafers and the blocking voltage of the chips.

The thermomigration also called “Temperature Gradient Zone Melting” [2] is a method allowing to create insulating p-walls through the wafer depth during a short time. The thermomigration is based on a recrystallization of semiconductor material with the liquid zone in the temperature gradient. As the zone moves it leaves behind a recrystallized trail of heavy doped p-type silicon the doping concentration of which is determined by the solid solubility limit at the operating temperature. Migration rate delivers up to tens of microns per minute at the migrating temperature 1000?1300°C. This process can yield through vertical p-n junctions at a much faster rate than conventional solid-state diffusion techniques. Lately the thermomigration is used in medicine, MEMS, solar cells etc.

As compared with foreign techniques our process of thermomigration differs by a number of features which permit to produce the high voltage chips up to 23?23mm in size on wafers up to 100mm in diameter. For linear zones pattern shaping the technique of the high-temperature selective wetting is used, based on dissolving of silicon by metal solvent in the windows was made by means of photolithography on an oxide or nitride mask. Such technique allows getting a pattern of sunken zones initially saturated with silicon. Juxtapositional resistive vacuum heating unit (Fig. 1) is used for thermomigration instead of IR-heated gas-filled gradient oven. Initial zones pattern was also changed.

Recently wafers (111) are commonly used for thermomigration because no linear zones orientation is needed in this case [2, 3]. For wafers (100) there are only two mutually orthogonal directions <011> and <0Ī1> of stable migration for linear zones. Otherwise in the course of migration zones are faceted at broken linear fragments on the exit side. It's clear that the rectangular pattern is the only possible for wafers (100).

Nevertheless, the migration rate for wafers (100) is almost twice faster than

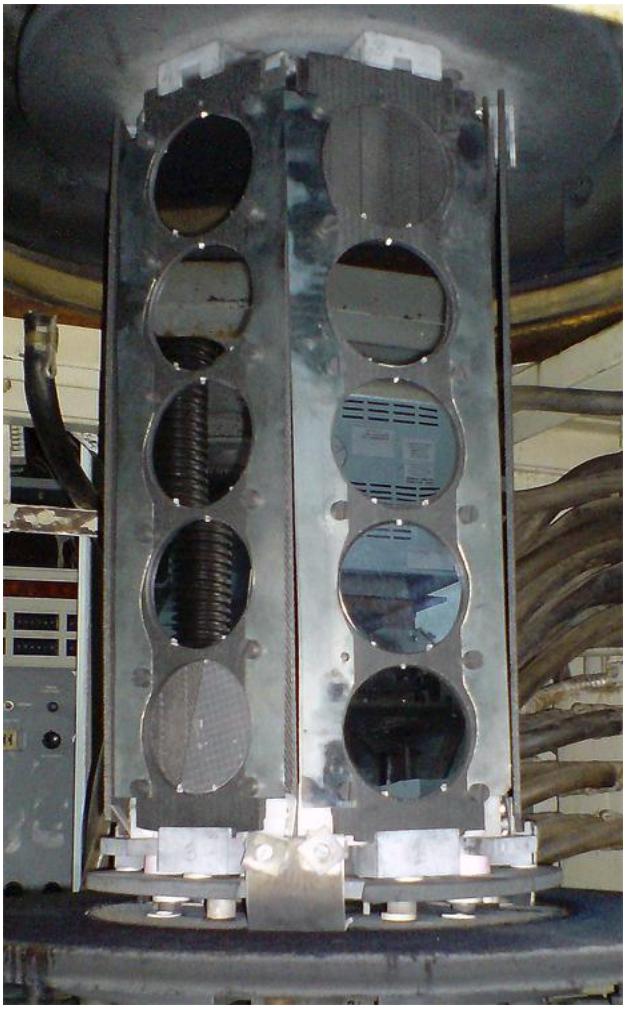

Fig. 1. *Juxtapositional resistive vacuum heating unit (30 wafers O76mm or 24 wafers O100mm)*

that for wafers (111). In addition the reverse blocking voltage of chips at the wafer periphery is almost the same as that of the central ones. This aspect becomes essential when chip's size and its blocking voltage are rising.

There is a drawback that only the rectangular pattern of zones is possible. As our experience shows, besides square shape the polyhedrons are also suitable for high voltage chips [7.10]. Thus the investigations of stable migration of non-oriented linear zones in (100) wafer at least 400-500 ?m in thickness is an important task.

Non-oriented linear zones migrated without faceting through (100) wafers in non-stationary thermal conditions with modulated IR heating [11, 12] when both direction and magnitude of temperature gradient was variable. These results were achieved only for zones formed by means of high temperature selective wetting. Zones which were formed by means of conventional vacuum deposition and photolithography in the course of migration were unavoidably faceted. One can explain these results by the fact that "wetted" zones are initially saturated with silicon atoms and a native interface oxide layer between zone and wafer surface is absent in this case.

Unfortunately meander-like carbon heaters of the gradient heating unit have a great thermal inertia (Fig. 1); therefore it is impossible to create non-stationary thermal conditions in this case. On that account the conditions of stable migration of arbitrary oriented linear zones through at least several hundreds of microns for (100) wafers were searched.

While comparing the data of different authors on the linear zones thickness, temperature and gradient magnitude one can make the conclusion that calculated zone thickness for all of them is almost the same and makes up 40-55 ?m. Therefore one may predict that the immersion

conditions are especially important for the further stable migration of linear zones through wafer (100). Analyses of stained zones tracks show that distortion of the migration trail is especially visible just after zones immersion into the bulk of semiconductor. Namely in this stage the stability of zones migration is minimal, because a normal component of the temperature gradient G_n near the wafer surface is far less than inside the wafer [13, 14]. Therefore, it's necessary to begin zones immersion at as high temperature as it is possible, when the influence of the anisotropy on dissolving is minimal. It is a temperature above of 1100?C when Al evaporation is essential. By the way, this task has no sense for the gas-filled IR gradient ovens, for G_n magnitude in these ovens is several times higher then in vacuum ones and zones immersion begins at comparatively lower temperatures, when the influence of the anisotropy is strong.

Stable migration through (100) silicon wafers was achieved for united pattern of linear zones [7]. Zones were formed on the entrance side of wafers with high temperature selective wetting. Their patterns were square, octahedron or circle. In the last case the auxiliary connective linear zones were used.

The linear zones were 80±2?m wide and 15-18?m deep, initial concentration of silicon atoms in zone was 22-26%. During the thermomigration the drive-in temperature made up about 1130°C. The highest operation temperature was 1180?C and after 10-15 minutes of soak it went down to 1130?C with a rate of about 0.5?C/min. All of the mentioned above patterns migrated stably through (100) Si wafers up to 520 ?m thick. The crystal perfection after migration was tested by etching of the samples in Dash etch. There was not any extra dislocation density both on entrance and exit side of the sample. However if lines were broken the open edge of zone while migrating was curved towards the {011} directions i.e. in accordance with the theoretical predictions. Simultaneously there was extra dislocation density around these edges. Besides there was not achieved any stable migration of non-oriented linear zones through (100) wafers if Al zones were formed by conventional vacuum deposition into grooves and photolithography even if initial zone thickness was 20?m.

2. DIODE CHIPS FABRICATION

To fabricate the chips of direct polarity diodes rated at 20A, 1600V, the float-zone (100) silicon wafers 37?39 Ω?cm, 290?m thick were used. These wafers had a lapped surface. The flat blocking p-n junction was formed in two stages. Prior to migration simultaneous diffusion of phosphorus on the entrance side and aluminium & boron on the exit side was made at predetermined depth (h_j=50?m). After the thermomigration the p-n junction was carried to 80?m during post-migration annealing. Then wafers were oxidized and anode blocking p-n junction was exposed by means of photolithography and mesa-etching on the entrance (cathode) side of the wafer. After following glass-passivation and metallization the reverse blocking voltage U_r for every chip was measured at leakage current less than 20?A. Every wafer of the batch was de bene esse separated at central and peripheral areas, and U_r was measured for "central" and "peripheral" chips separately. $\bar{U}_r$ magnitude for central chips in the batch was 1685.6 V and for peripheral ones it was 1746.9 V. The

histogram for both these subbatches is shown at Fig.2

Yield percentage of the suitable chips made up 87.9% and the amount of low

mesa-groove depth from center to wafer edge. However for (111) wafers central chips every time have higher blocking capability of vertical p-n junctions.

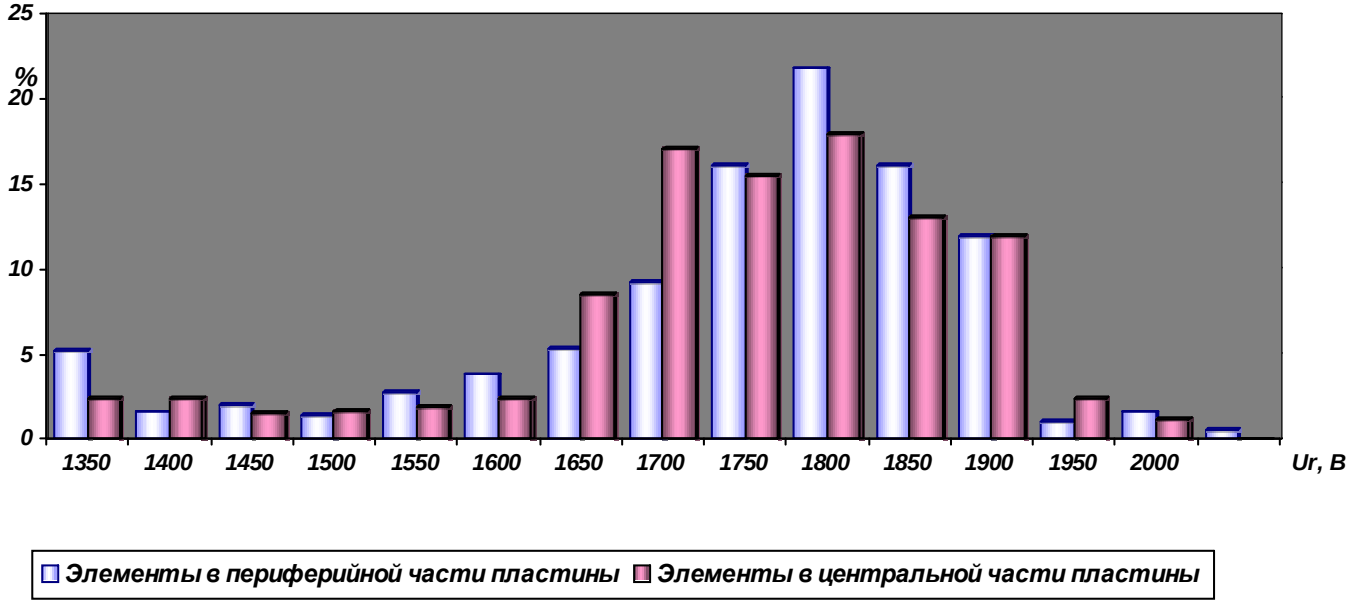

Fig. 2 *Histogram of U_r distribution for direct polarity diode chips situated at the central part (bright) and at the periphery (dark) of the (100) wafers.*

class chips was considerably little. This result shows that (100) silicon wafers are suitable for fabrication of high voltage chips by means of the thermomigration.

Distinctive feature of this result is that peripheral chips at (100) wafers have a higher blocking voltage as compared to central part of the wafer. It was unexpected and it's unattainable for (111) wafers as our experience of fabrication of chips of different sizes shows. Also we find it very interesting that p-trial local deviations in (100) wafers are not connected with U_r worsening, however it is well known that any deviation of zone path from normal to wafer surface leads for worsening of blocking capability of vertical p-n junction of p-wall [2]. Maybe it is connected with the randoming of

3.HIGH-CURRENT DIODE CHIPS FABRICATION

Diode chips 14?14mm and 20?20mm were fabricated for modules rated at 100A and 200A correspondingly. Chohralsky n-silicon (100) wafers 20 Ω?cm, 300_{-20} ?m thick and 76 mm in diameter were used. Wafers surface was lapped. Chips had a square shape. Linear doubled zones [6, 9] with cut corners were joined in united pattern. This pattern was not oriented. The technological route was the same as it was mentioned above [15]. Exit side of the wafers after thermomigration is shown at fig. 3.

After the thermomigration and post-migration diffusion annealing the flat

blocking anode p-n junction was 95?m deep. Annealed doubled vertical p-walls were 460-470?m wide. Glass-passivated mesa-groove at the cathode (entrance) side was 100-110?m deep. U_r values were 960-1130V in accordance with instant n-silicon resistivity and $\bar{U}_r$ magnitude for "central" chips was 6.5% less than that for peripheral ones as it was for 20A chips mentioned above. These chips were used in modules МДД8/3-200. For minority carriers lifetime τ_i in instant silicon was less than 10?s, τ_i in diodes was also less than 10?s and forward voltage U_f (I_f=200A) was 1.29±0.03V in accordance with technical datasheet.

Circular diode chips O24mm were fabricated at (100) Si wafers 70 Ω?cm. Zones pattern shown at fig. 4 was designed in accordance with [7] including auxiliary lines. U_r value for these chips was above 2.2 kV

SUMMARY

It was shown that stable thermomigration of complete patterned non-oriented linear zones through (100) silicon wafer in stationary thermal mode is possible. Conditions sine qua non are complex initial zones patterning, the method of zones forming when zones are initially saturated with silicon and also the thermal-temporary mode of immersion and migration. This process allows to fabricate reproducibly the chips with high U_r values both in the centre of the wafer and at the periphery. Thus the thermomigration through wafers (100) has proven to be an effective means in fabrication of high-voltage chips having large square, complete shape and high

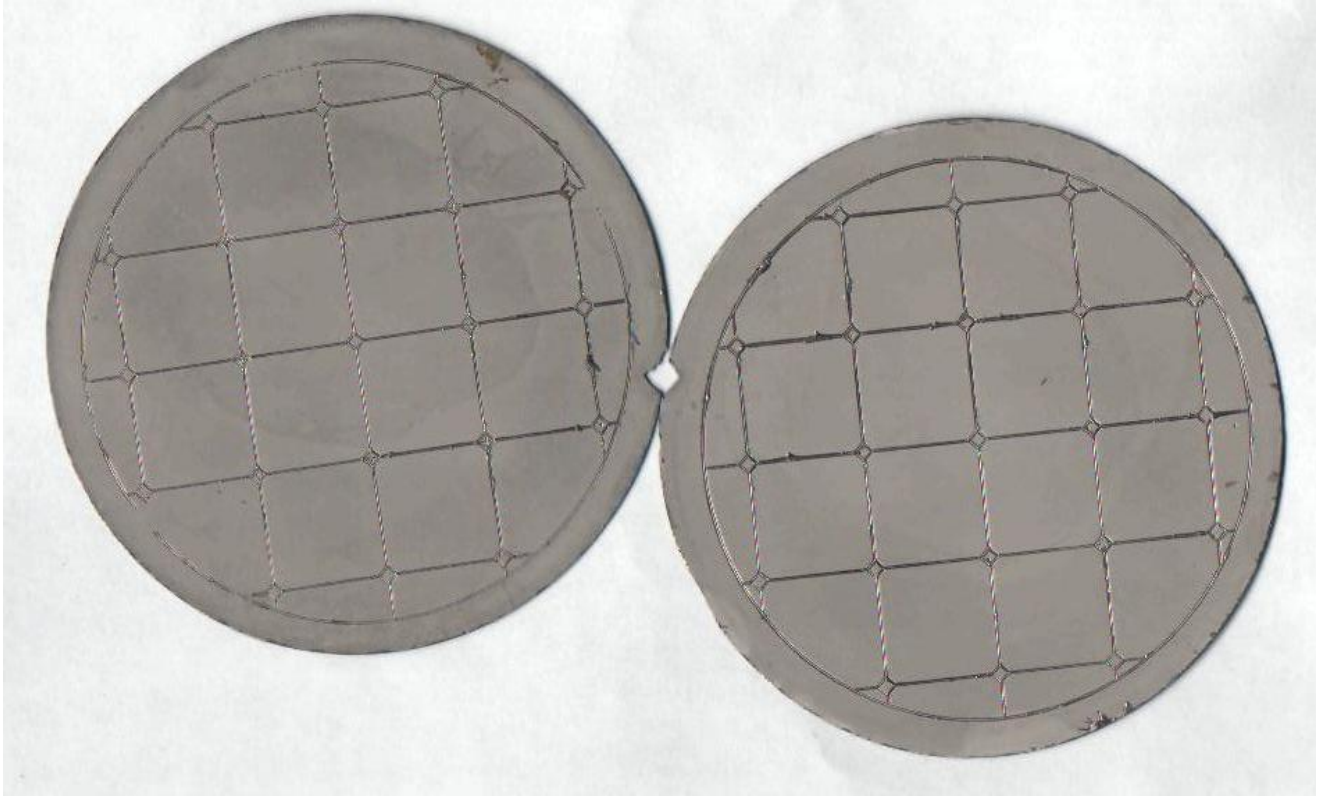

Fig.3. *Exit side of (100) wafers after thermomigration. Breaks at the wafer edges permit to estimate pattern orientation according to {011} directions.*

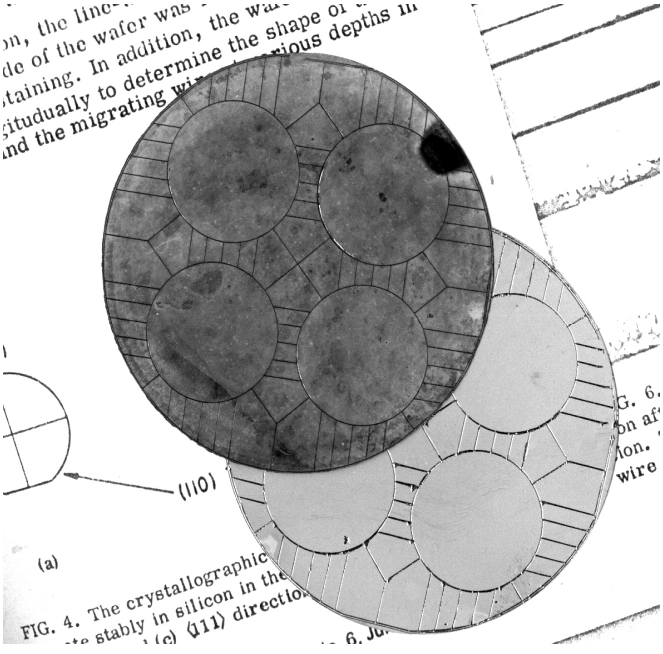

Fig. 4. *Exit side of (100) wafers after the thermomigration (right) and after staining (left) against the background of article [3].*

grade homogeneity properties of vertical p-n junctions regardless from their orientation.

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