APPLICATION of the THERMOMIGRATION
for POWER SEMICONDUCTOR DEVICES TECHNOLOGY

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One of the basic tendencies of the power semiconductors development is substitution of discrete devices in hermetic glass-to-metal packages for modules, where the structures of power semiconductor devices (thyristors, triacs, transistors, diodes etc.) are soldered on an insulating ceramic substrate and encapsulated into a plastic case. These structures fabricated by world productors have one-sided passivation; anode blocking p-n junction is exposed on the upper surface of the structure through the peripheral separating area, so called, vertical insulation. Such structures are more reliable as compared to structures with double-side mesa [1] and allow direct soldering on a metallized ceramic substrate without thermal compensator. That's why the tendency of increase of modules current and growth of blocking voltage was designated.

Well-established solid-state diffusion is used for making of vertical isolation by the majority of manufacturers as the most mastered process. The square-law dependence between diffusion term and p-n junction depth essentially lengthens the process of deriving of a vertical isolation on thick wafers of high-ohmic silicon used to manufacture of high-voltage devices, so electrophysical parameters of the initial silicon are changed for worse.

The thermomigration or temperature gradient zone melting is a method of through-wafer local doping of silicon [2-4]. The liquid zone of molten solution migrates through silicon along a temperature gradient, leaving a recrystallized "track" doped by atoms of the metal - dissolvent (aluminum) up to a solubility limit at the processing temperature. Thermomigration allows to reduce the fabrication term of through vertical isolation up to tens minutes, since in practical cases the rate of migration reaches units or even of tens of micron per minute at the processing temperature 1200-1260°C. Recrystallized areas along wafer depth have an approximately identical concentration level of an acceptor dophant and perfect crystalline structure [2]. The thermomigration is combined with conventional technological operations of semiconductor processing: diffusion, photolithography, and epitaxy.

Before thermomigration technology development started at our firm, the stage of publications and intensive licensing of technique, equipment and application of a method both in our country and abroad was replaced by the stage of internal know-how improvement for those, who are skilled-in-the-art. The characteristic features, mutual for well known manufacturers, were: using of wafers, having polished surface with orientation as a rule (111); a grid-like pattern of linear aluminum zones formation on a surface of wafer by conventional vacuum deposition of thick aluminum layer followed by photolithography and etching. The thermomigration is carried out in gas-filled gradient furnaces having one-sided heating by IR lamp compartment, with horizontal layout of wafers. After-thermomigration wafer treatment includes lapping and polishing [3, 4]. It was announced that such a process with the thermomigration allows manufacturing 1Ч1 mm chips having reverse_blocking voltage less than 600 volts [4].

In domestic power semiconductor technique usually the wafers with the lapped surface are used. The problem is that the zones is obtained by E-gun evaporation and photolithography, are

not immersed from the surface into the lapped surface, as it happens to the polished one. The difficulties of immersing for such linear zones are explained also by discrepancy between low-temperature deposition processes versus high-temperature thermomigration process, even if the zones are deposited into grooves etched previously. For discrete zones pattern shaping the technique of high-temperature selective wetting [5, 6] is used, based on dissolving of silicon by melt of the metal - solvent in the windows created by means of photolithography on an oxide or nitride mask. Such method allows getting a pattern of initially saturated with silicon sinken zones of required topology on a wafer surface.

The thermomigration process is carried out in vacuum. Vertically located wafers are exposed to one-sided resistive heating [2]. The wafers are allocated in the holes of carriers installed around exterior edges of the prism-like heating block. To provide a uniform temperature gradient field over the area of wafers being processed we use meander-shaped carbon composite material heaters. Such technique [6, 7], was worked out with the help of the scientists of Novocherkassk Polytechnic Institute, all the equipment was created by the designers of Zaporozhye VNIIpreobrazovatel; it allowed to treat wafers with a diameter up to 76 mm, from 250 to 750 microns thickness with a yield on the thermomigration operation more than 95% for square structures of power silicon devices (diodes, thyristors, triacs, light-controlled thyristors etc.) having side dimension up to 5.2 mm. The main characteristics of heating methods used at thermomigration are represented in the following table

Table

IR heating in non-oxidizing gas atmosphere	Resistive heating in vacuum
1. Simplicity. It is enough to modernize the rapid thermal annealing furnace	1.Juxtapositional vacuum thermal chamber with program control is used
2. Rigid requirements to admissions, quality of manufacturing and adjustment of details of the equipment.	2. Requirements under admissions for the majority of details are not rigid.
3. Fast heating and cooling are possible	3. Rate of heating and cooling are defined by thermal inertia of thermal unit
4. The value of a temperature gradient exceeds 150°C/sm, migration velocity is high.	4. Values of a temperature gradient and Migration velocity are moderate. Additional time for getting of vacuum the chamber is required.
5. Single-piece wafers processing.	5. Group processing of wafers with cassette loading.
6. Products of migration remain on a wafer surface, and it is necessary to remove them	6. Aluminum evaporates from a finish surface of wafer during process.
7. Specific power consumption is high (for a wafer ∅4" it is spent 5-7 kWhr)	7. Specific power consumption is moderate (1-1,5 kWhr for a wafer ∅4")
8. It is used for manufacturing of thyristor chips 1 × 1mm, rated for voltage up to 600V, on rather thin wafers	8. It is used for manufacturing of thyristor chips up to 20 × 20mm and ∅20 mm, having voltage up to 2000V. Wafer thickness is unlimited.

During development of devices on currents more than 100 A and voltage more than 1600 V, a lot of problems arose which were not essential earlier for small structures. It was necessary to eliminate zone breaks and ruptures during zones forming by selective wetting and thermomigration. Besides the special value has homogeneity of physical properties of isolation for whole perimeter on chips with large perimeter of a vertical isolation, in particular, blocking capability of vertical p-n junctions. In its turn it is strictly connected with migration stability of extended linear zones, absence of its local curvatures and thickenings.

With the increase of chip size and decrease of the amount of chips on a wafer each break of a zone wastes greater percentage of the wafer surface. The integrity violations of linear zones at its forming are connected not only with photolithography fault, but also may be caused by local shadowing of windows in the mask with foreign particles, presumably, Al_2O_3 scales by a size less than 100 microns. As the main breaks quantity caused by shadowing, is dated for area of primal wetting, the topology of photomask is changed. On wafer edge, where the structures are absent, the concentric edge zones are entered. During zones forming the scales remain on the edge zones in the area of primal contact. It allowed to eliminate violations of zones, forming vertical isolation of structures.

A uniformity of blocking capability of vertical p-n junctions along each structure perimeter, the absence of points with increased leakage current along a perimeter of vertical p-n junctions defines a degree of the thermomigration perfection and restricts, eventually, the sizes of structures, which can be manufactured at this level of technology. Such uniformity is defined, besides the breaks of zones at forming, also by the absence of distortions of zones trajectory. The reasons of migrating zones trajectory motion aside from normal to wafer surface are:

1. Caused by tangential component of temperature gradient G_τ, on the magnitude, comparable on the order, to its normal component G_n.
2. Connected with zones instability at imbedding stage.
3. Stipulated by the anisotropy of crystallographic properties of silicon.

The tangential component of temperature gradient G_τ on a wafer periphery caused by net radiation losses from edges of a wafer, can be suppressed with a wide (500 microns) ring zone located near a wafer edge [8] or opposing radiation from a hole of the thick silicon carrier [4]. In our case besides compensating radiation from the hole in graphite cassette the effect of thermal compensation from edge zones that migrate simultaneously with structures forming zones is used. These zones are auxiliary at zones forming, as it was mentioned above, and during migration they suppress G_τ at peripheral areas of a wafer. Geometrical parameters of these auxiliary zones are the same, as well as for the basic zones; therefore they act as G_τ suppressor during all the migration process.

Discrete zones imbedding into a bulk of silicon is the most critical stage of the thermomigration process [2,9], as the G_n magnitude on a wafer surface is lower as compared to the bulk, especially at rather low temperatures [9,10]. Complete zones imbedding on the entrance surface of a wafer doesn't occur simultaneously for different fragments of zones. Time randoming can reach 500 seconds even for single 76 mm wafer. It depends on crystallographic orientation of the wafer and zones geometry especially in zones cross-sections on entrance side. Reducing of an imbedding term randoming is achieved by means of connection of zones pattern as unified "band", even if these zones are not located adjacently with each other. The special requirements are produced to photomasks in places of linear zones intersections. In these places enlarged diagonal dimension of zones occur and imbedding is hampered. In Figure **1** the track of the imbedded intersected zones on silicon with orientation (111) (a) and (100) (b) is shown. One can see that for silicon with orientation (111) imbedding in intersection is hampered, which is indicated by the size of a hollow with characteristic faceting by planes (111). Zones are immersed faster into a wafer with (100) orientation and the delay for them on entrance side of the wafer is less. It may be explained by faceting of "hot" (dissolving) zone border [2]. In Figure **2** the exit side of the same wafers after the exit of zones on a surface is shown. The distortion of a zone shape in intersection for silicon wafer with orientation (111) is more noticeable and it is determined, as it was already told, by the delay of a zone at start in its local widening, in this case, in intersection.

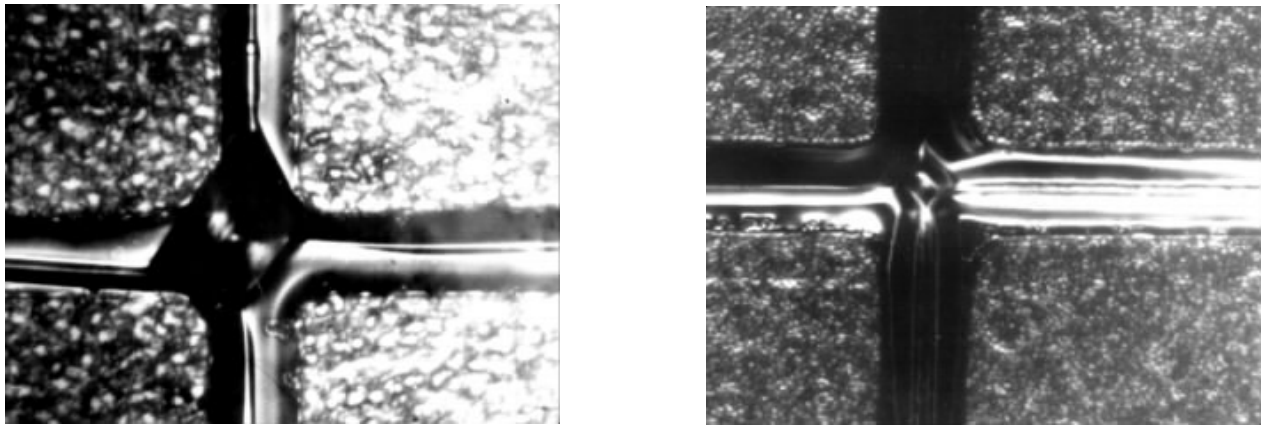

Figure 1 – Zones cross-section on silicon wafer with (111) (a) and (100) (b) orientation. Entrance surface. 100×

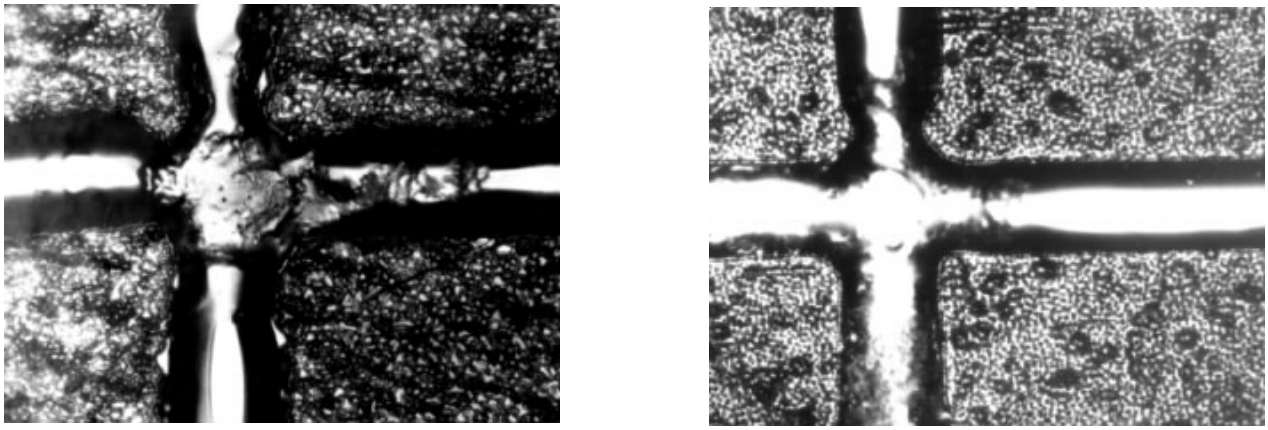

Figure 2 – Zones intersection on exit surface of a wafer with (111) (a) and (100) (b) orientation after an exit of zones.100×

Conventionally in thermomigration technique for SCR application silicon wafers with orientation (111) are used since they do not require linear zones orientation [2]. For silicon with (100) orientation as directions of stable migration the directions {011} were considered only orthogonally related, which required initial orientation of zones strictly along these directions. However, silicon wafers with orientation (100) allow to receive structures with higher blocking voltage, as compared with (111) orientation silicon having the same specific resistance. In many respects it is explained by easier imbedding of zones into silicon (100) so zones migrate without distortions. From three components of thermomigration (dissolution of silicon on the “hot” boundary of a zone, diffusion of silicon atoms through a molten solution and crystallization of them on the “cold” boundary) the first is the most critical [2]. The mutual influence on each other of the both zone boundaries reduces migration rate, especially for considerably thin zones, in a so called kinetic mode [2] that is especially noticeable during zones imbedding, when the temperature gradient is small, and the anisotropy of crystallographic properties of silicon has an effect. If zone thicknessis scanty it can deflect from a normal to a wafer surface just after imbedding of silicon with orientation (111). This effect is almost negligible for gas-filled chambers with effective heat sink,ofor temperature gradient magnitude in this furnace is higher then for vacuum one.

However vacuum furnaces have some advantages. They are more economical and can make the process conditions close to equilibrium ones, which provide for perfect crystallography of recrystallized isolating zones and vertical p-n junctions. They have blocking voltages up to theoretical limit even without post-migration annealing.

After thermomigration in vacuum 10^{-4} mm. Hg occurs the aluminum zone evaporates. The necessity of products of migration etching after completion of the process disappears. During thermomigration in vacuum the doping of wafers by aluminum from vapor is carried out. For a local doping the mask of sufficient firmness is used [11].

The new topology of separating areas is adopted. The structures are separated with two parallel zones. In the vicinity of intersections zones width smoothly diminishes at 10 %, so a diagonal size of zones in intersections decreases. In its turn, it makes zones imbedding in intersections easier. All zones - both basic, and edge - are incorporated as a uniform system by connective zones and their motion through a wafer is synchronized being connected during its entire driving path. Zones parameters (width and distance between parallel zones, and also migration condition) are selected in such a way that in the interval between structures the area with dislocated crystalline structure is formed and it acts as a getter during consequent thermal operations. In Figure 3 the area of intersection of linear parallel zones is shown, which width smoothly diminished to intersections.

The migration of parallel adjacent zones is more stable, than of single zone. Besides even if one of two zones breaks one of two adjacent structures will leave fit. The decrease of local widening in zones intersections has allowed facilitating imbedding band of linear zones. Imbedding delay time dispersion [9] on a wafer 76mm in diameter is reduced more, than twice. The aberration from a normal to wafer surface for a track of migration in a parallel way migrating adjacent zones diminishes too.

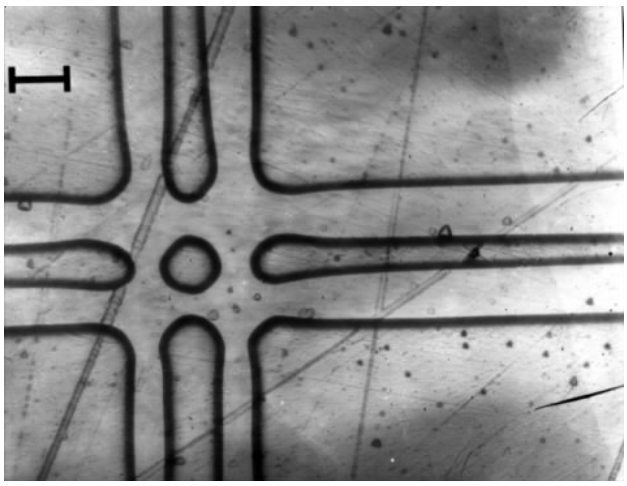

Figure 3 – Intersection of the doubled zones. Exit surface. 100×

New technological route eliminating the operation of grinding of wafers after thermomigration is offered [12]. For SCRs (thyristors, triacs etc.) the diffusion will be carried out in two stages - before the thermomigration and after it. Additionally wafers are doped with aluminum during thermomigration processing. For direct polarity diodes diffusion is also carried out in two stages [14].These changes, and also the change of operations order of the conventional technological route, have allowed to increase both common yield and high-voltage structures percentage.

In Figure 4 the histograms of class distribution of glasspassivated 100A diodes of direct polarity is shown. Besides the diodes with thermomigration (solid line) the class distribution for conventional beveled diodes of direct polarity is represented. Both batches are manufactured from silicon of the same ingot. The diffusion on both batches was carried out simultaneously. The structures were tested with an automatic tester permitting to arise reverse voltage no more than 2000 V.

Apart from saving of silicon by means of handling initially thin wafers (without a rough tolerance on lapping after thermomigration) and increase of common yield it was possible to achieve high reproducibility of structures parameters on a wafer and in a batch of treated wafers. For SCRs it has appeared possible to modulate the concentration profile of horizontal diffusive layers depending on the device assignment and on combination of sensitivity to gate signal and dynamic properties, necessary for the customer.

The application of local masking during thermomigration has allowed to combine in a single technological route the creation of isolation by thermomigration with the field guard rings forming. This combination permits to increase SCR blocking capability.

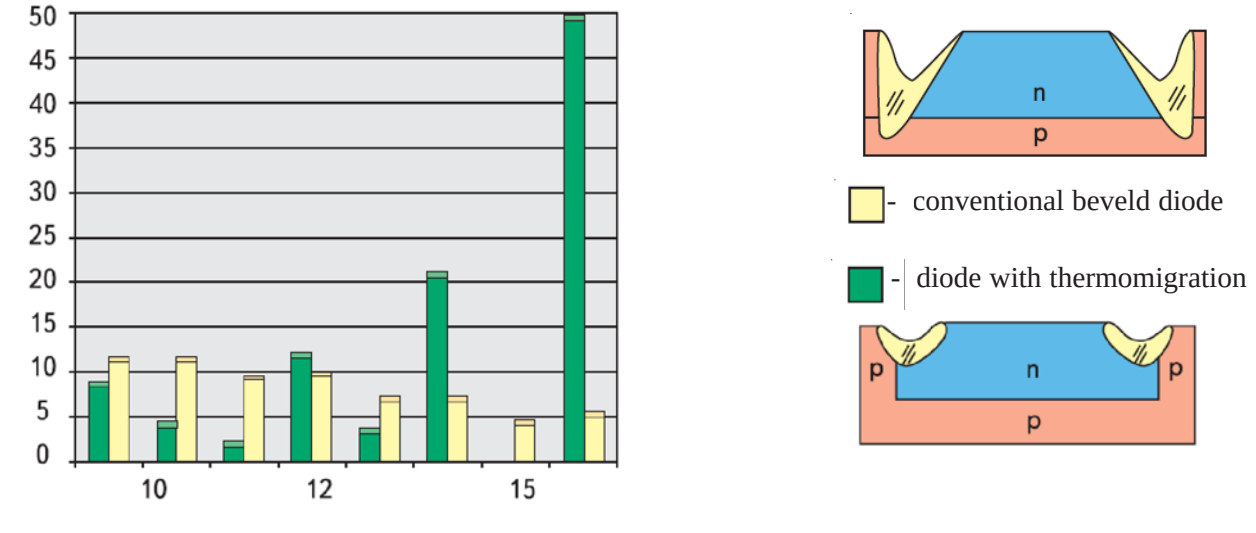

Figure 4 – Distribution on classes of diode structures Д140-100: with mesa-planar and conventional bevel both passivated by glass.

Improvement of the technological route of manufacture glasspassivated structures and improvement of thermomigration processing and zone patterning allow to develop the series of power silicon devices on current more than 100 A: thyristors, light-controlled thyristors, diodes etc. - for a complete set of high-voltage power semiconductor modules creation.

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